# A New Logic for Implementation of Digital Error Correction Block

# Abstract:

This paper proposes a novel architecture for the digital error correction logic block that is used in pipeline analog-to-digital converters. The new architecture is implemented with HA and OR\_HA blocks instead of HA and FA in the conventional architecture. This architecture for digital error correction logic is simulated in 0.18μm CMOS process by using Cadence. The simulation results show that the proposed architecture improves speed and power consumption. Also this architecture occupies less area than the conventional digital error correction block.

**Tools used:**

**Tanner**